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Spur Reduction Of MB-OFDM UWB System using CMOS Frequency Synthesizer

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***Abstract*- As Technology progress deeper into submicron CMOS, traditional analog circuits face problems that are not to be solved purely by analog innovations. Instead, new architectures are being proposed which take advantages of the relatively cheaper of the digital circuits to augment or improve the diminishing performance of the analog circuitry. The conventional approach performs the design of 14 bands CMOS frequency synthesizers with spur reduction for MB-OFMD for analog circuits which have high distortions and noise. My proposed work is to replace the analog input PLL into All Digital PLL with spur reduction. Then the frequency mixing architecture alleviates harmonics mixing and pulling to diminish spur generation. The simulation is performed using Model SIM and the implementation using Microwind to diminish spur reduction.**

***Index Terms*- ADPLL, CMOS frequency synthesizer, Digital PLL, spur, Mixer, Multiplexers.**

I. Introduction

Many circuits currently face the problem of clock skew, and registers and flip-flops are not receiving the clock at the exact same time. The clocks are generated by oscillators, but the clocks that reach the registers and flip-flops are distorted and require a phase locked loop to address this problem. A phase locked loop ensures that the clock frequencies seen at the clock inputs of various registers and flip-flops match the frequency generated by the oscillator. The phase locked loop (PLL) is a very important and common part of high performance microprocessors[4]. Traditionally, a PLL is made to function as an analog building block, but integrating an analog PLL on a digital chip is difficult. Analog PLLs are also more susceptible to noise and process variations. Digital PLLs allow a faster lock time to be achieved and are attractive for clock generation on high performance microprocessors. The all digital phase locked loop was designed such that it is composed of four main components. The components are analogous to the analog PLL, but the implementation consists of digital components. A digitally controlled oscillator (DCO) was utilized instead of a voltage controlled oscillator. As proposed by multi-band orthogonal frequency division multiplexing (MB-OFDM) alliance, the spectrum for ultra-wide band (UWB) communication system ranges from 3.1–10.6 GHz, which is divided into 14 bands with each band of 528 MHz and categorized into five groups[1]. According to IEEE 802.15.3a recommendation, the frequency hopping time for band switching should be less than 9.5 ns. It provides 480 Mbps for WPAN application. To meet the stringent frequency hopping time requirement, several frequency synthesizers based on single-side band (SSB) frequency mixing were proposed.

Nevertheless, these architectures demand multiple phase-locked loops (PLLs) or sophisticated dividers to provide adequate sub-harmonics for the full band frequency synthesis. For 14 bands carrier generation[2], the prior art in the literatures requires three stages cascaded SSB mixers in the signal chain or employs an external voltage control oscillator (VCO) instead of an integrated PLL. As a consequence, they are susceptible to in-band spurs generation, harmonic pulling, and encounter difficulties in I/Q carrier generation.

II. System Architecture

This paper proposes a new modified PLL overcoming the analog PLL limitations. The analog and digital PLL are classified into existing & proposed systems.

A.Analog PLL system

Fig.1 shows the proposed 14 bands frequency synthesizer architecture, which is composed of only one PLL, two stage SSB mixers (three pairs for I/Q operations), and two stage multiplexers.The PLL is operated at 8448 MHz, providing I/Q phases from a LC-QVCO, and phase-locking to an external 264 MHz reference. The frequency planning for the 14-band carrier generation is shown in Fig. 2, which is categorized into two folds,

$$f_{LO1}=264 \times (16\pm k)$$

$$f_{LO2}= 264 \times (32\pm k)$$

where $K \in \{1,3,5,7\}$.

Here f_{LO1} generated by SSB Mixer2 covers the carrier generation for band 1 to 6, and f_{LO2} generated by SSB Mixer3 covers band 7 to 14. As the divider chain in the feedback path is composed of 5 stages divide-by-2 dividers, the 4224 MHz I/Q carrier is available at the output of the first stage divider, while the even order harmonics (8th, 4th, and 2nd) of 264 MHz can be derived from the 2nd to the 4th stage dividers. The odd order harmonics (3rd, 5th, and 7th) of 264 MHz are then indirectly synthesized from the reference frequency (264 MHz) and its even order harmonics, which are performed by

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SSB Mixer1 and MUX1. In order to achieve broad band operations while relaxing the complexity of signal routings, the full 14 bands, (Group 1, 2) and (Group 3, 4, 5), are then derived by mixing the odd order harmonics of 264 MHz (1st, 3rd, 5th, and 7th) with 4224 MHz and 8448 MHz respectively.

They are performed separately by the 2nd stage SSB mixers, where SSB Mixer2 is employed for f_{Lo1} and SSB Mixer3 for f_{Lo2} generations. The inactive 2nd stage SSB mixer will be shut down to save power and provide better side band isolation. Finally, the output carrier is picked up by MUX2 and delivered into the output buffer.

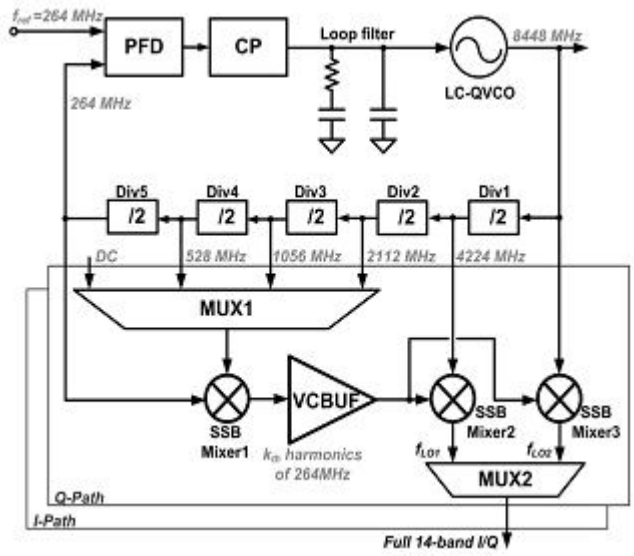

Figure. 1 Fourteen Bands Frequency Synthesizer Architecture For MB-OFDM Transceiver

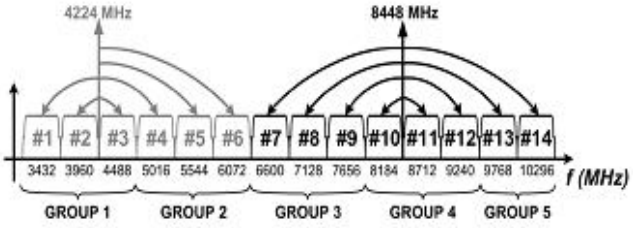

Figure. 2 Frequency Planning For 14 Bands Carrier Generation

A charge-pump based PLL is adopted for generating the harmonics of 264 MHz. The PFD in this design incorporates true single phase clocking(TSPC) D flip-flop with combinational logic for higher resolution. The core circuit of the charge pump is shown in Fig.3, which is basically composed of current steering switches (M1–M4) and pumping current I_{U2} and I_{D2}[3].

As the terminal voltage of the LPF is approaching the rail potential (V_{DD} or ground), the pumping up and down currents (I_{U2} and I_{D2}) will become unbalanced due to the channel length modulation effect. This will result in unequal up and down pulse width in the locked state, and thus induces reference spur.

The PLL output spectrum at 8448 MHz is shown in Fig. 4.The output power is about 12 dBm after the cable loss is taken into account. The reference spur at 264 MHz offset is

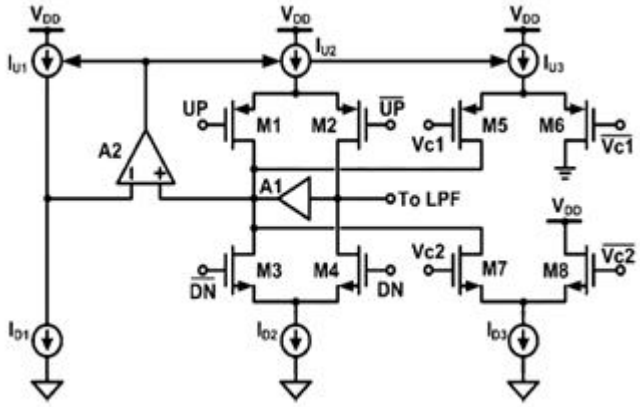

Figure. 3 Charge Pump Circuit

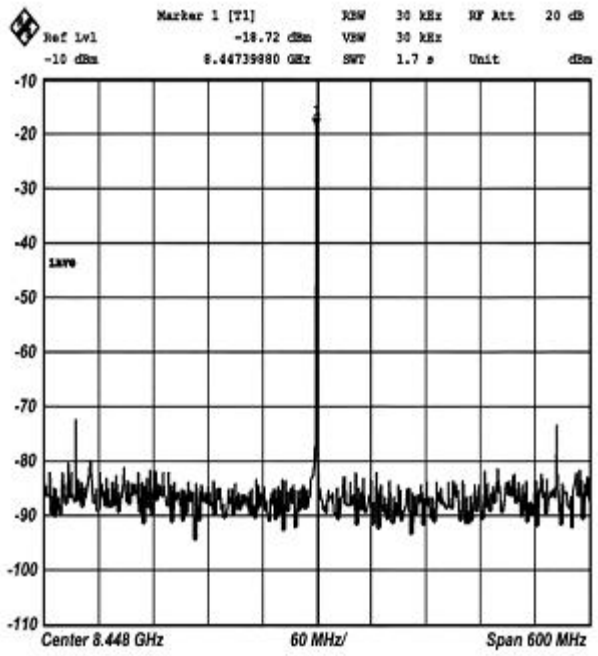

Figure. 4 Measured PLL Output Spectrum

lower than 55 dBc.

B. All Digital PLL system

The All Digital PLL system deals with the full of all digitally components where it overcome the limitations complexity, noise distortion of analog PLL.The ADPLL(All Digital PLL) is a cheaper circuit than the analog PLL.Fig 5. Shows the block diagram of digital PLL. The Phase Frequency Detector (PFD) detects the phase and frequency mismatch of the reference clock and divided DCO clock.

The PLL is locked when the PFD detects that the phase and frequency of the two clock inputs match. The output of the PFD drives the time to digital (T2D) converter. The PFD produces up and down enable signals that are interfaced to the T2D converter. The DCO clock is divided by a specific multiplication factor, in our case it is four, and sent back to the PFD for phase and frequency comparison. The main components and their implementation will be discussed in the following sections. The implementation of the entire PLL contain VHDL based components and the simulation part is

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done in Model Sim[6].

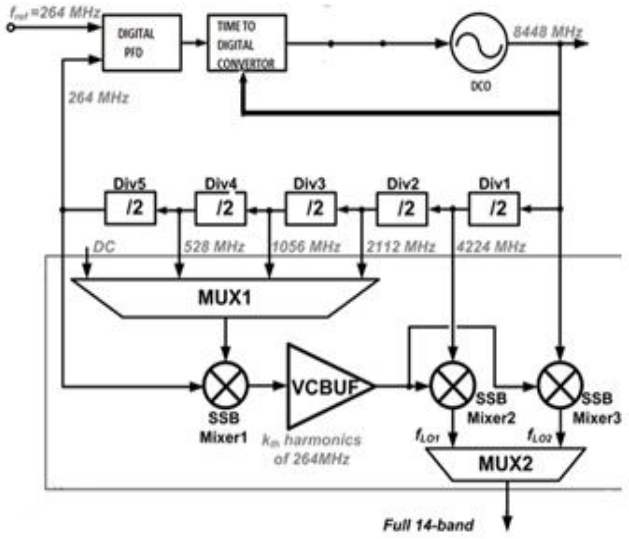

Figure.5 Block diagram of ADPLL

1) Design Of ADPLL System Components

(i) Digital Phase/Frequency Detector

The phase frequency detector is a significant aspect of the PLL because it determines whether the reference clock and divided DCO clock are in phase and are running at the same frequency. The design used is shown in Fig. 6. A modified D Flip-flop was utilized because the D input doesn't change and remains high always.

The output of the modified D Flip-flops enters a two input NOR gate that resets the Flip-flops if both clocks are high. The up and down signals indicate if the DCO clock needs to be increased (up is true) or decreased (down is true). The event and direction signal are necessary to create the up and down enable signals for the T2D converter[5]. Additional circuitry between the PFD and T2D is required for the signal conversion to take place.

The design and understanding of the PFD was important when continuing with the design and implementation of the other components of the system.

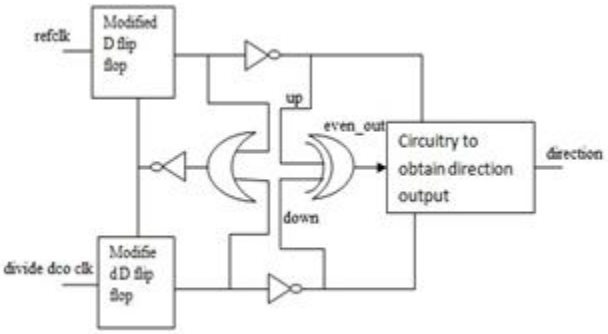

Figure.6 Phase Frequency Detector Diagram

(ii) Time To Digital Convertor

The time to digital converter consists of a 6 bit down counter, 6 bit up counter, and 6 bit carry ripple adder. The phase detector controls the up counter and down counter by up and down enable signals. The initial state of the up counter is "000000" and the down counter is "111111."

The up counter and down counter values are input into the six bit adder and the output produces the seven bit control word for the DCO. Fig. 7 shows the connections of the T2D converter. The six bits from the adder and the carry out bit compose the seven bit control word. The converter should be active only if there is a phase and/or frequency mismatch. Clock gating has been performed to disable the T2D when both the reference clock and divided DCO clock are locked.

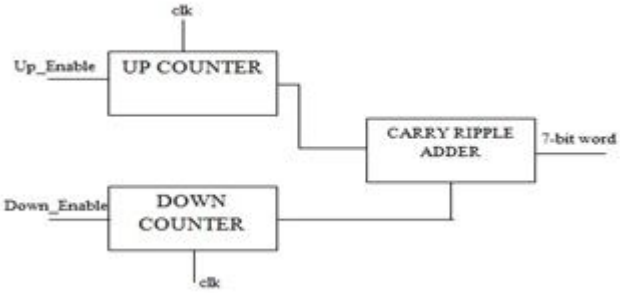

Figure .7 Time To Digital Converter Diagram

The outputs from the carry ripple adder emerge at different times. In order to correct this error, a register made of D flipflops was used to store the outputs from the adder. The seven bit control word was released from this register based on the clock given to the counter, delayed by an amount equal to the propagation delay of the counter and the adder.

(iii) Digital Controlled Oscillator

An optimized DCO was developed to be analyzed with regard to power, but due to time limitations this was not performed. The optimized DCO should have consumed less power and resulted in a more energy-efficient PLL. The digital controlled oscillator removes the jitter in the given frequency. This DCO is easy to make using standard cells, but its power consumption is quite high.

(iv) Frequency Divider

The output of the DCO needs to be divided to match the reference frequency. The implementation contains a divide by four frequency divider, enabling the PLL to have a multiplication factor of four. The divider is implemented by using two series D Flip-flops. The DCO clock is input into both flip-flops and the non-inverted output of the second flip-flop is the DCO clock divided by four.

III. Experimental Results

The Experimental prototype of UWB system synthesized in VHDL components and the simulation output is implemented in Model Sim.

Here they are two types of conditions exist one is the locking condition and another one is the unlocking condition.The locking condition shown in the Fig.8.The fig.8 shows that the reference clock and feedback clock matches with the frequency of 4 GHz range with the locking condition indicates as in yellow strip and the frequency divider divides the clock with division of 5bit(00000101).After finishing the division, the reference and feedback clock start locking condition with the frequency matching.

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Figure. 8 Locking Condition Under 4 GHz

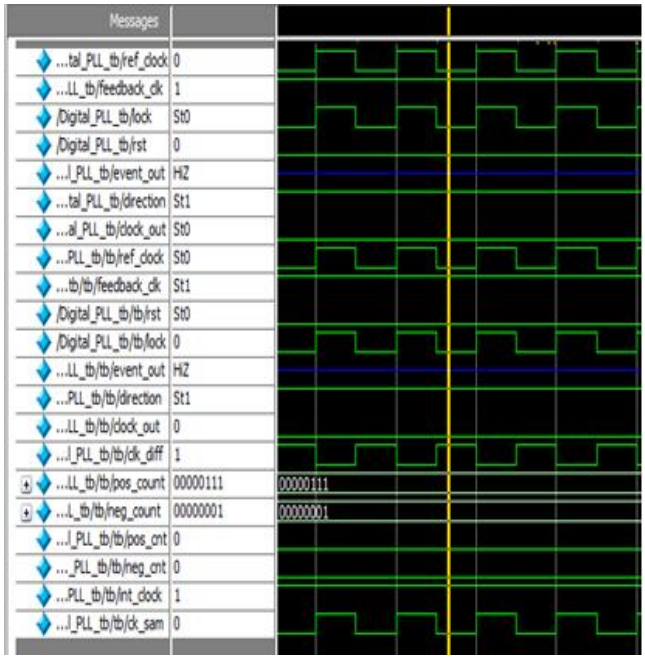

Figure.9 Unlocking Condition Under 0.2 GHz

The unlocking condition shown in the Fig.9.The fig.9 shows that the reference clock and feedback clock doesn't matches with the frequency of 0.2GHz range with the unlocking condition indictes in the yellow strip and the frequency divider divides the clock with division of 7 bit(00000111). After finishing the division, the reference and feedback clock start the unlocking condition with the frequency matching.

The locking condition with spur reduction shown in the Fig.10.The fig.10 shows that the reference clock and feedback clock matches with the frequency of 0.2 GHz range with the locking condition and the frequency divider divides the clock with division of 252 bit(11111100). After finishing the

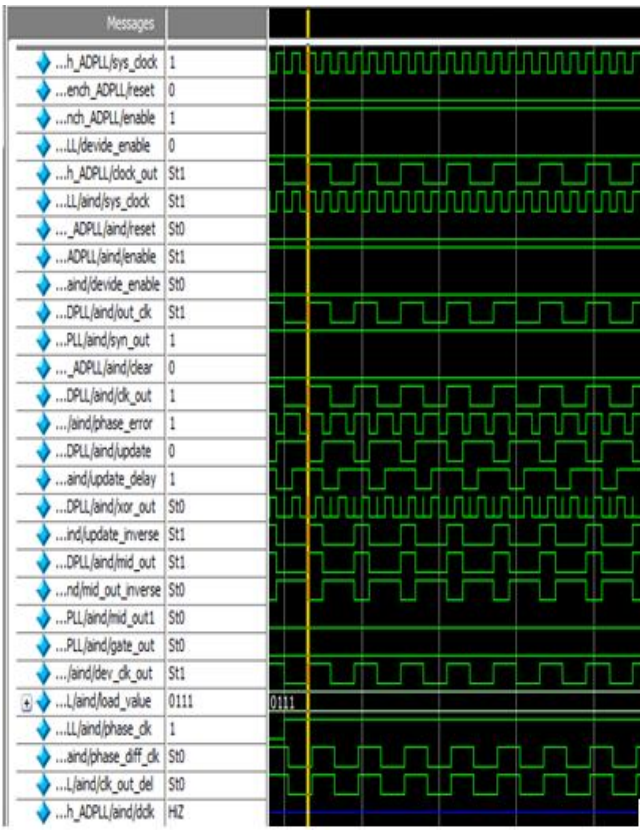

Figure.10 Simulation output in locking condition with Spur Reduction

division, the reference and feedback clock start locking condition with the frequency matching.Then the multiplexer and mixers start removing the spur indicated by yellow strip line as xor_out.Thus the spur is reduced at 5030 ps.

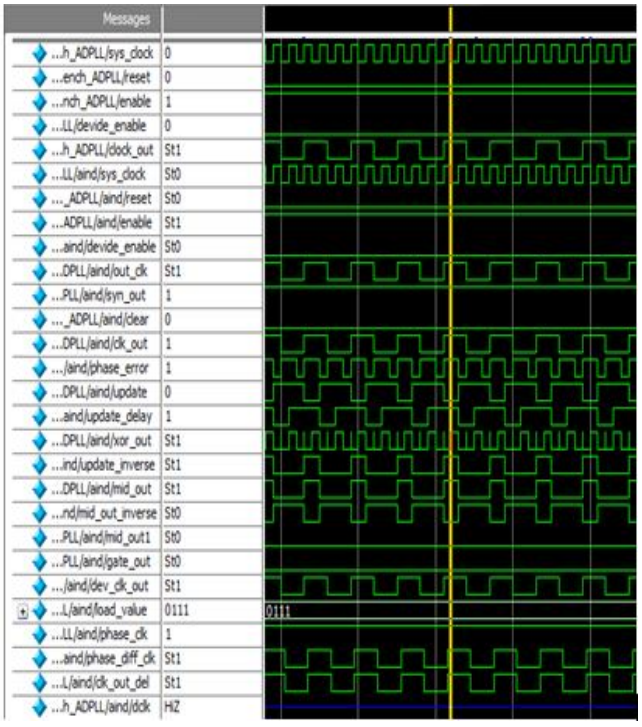

Figure.11 Simulation output in un locking condition with Spur Reduction

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The fig.11 shows that the reference clock and feedback clock matches with the frequency of 1 MHz range with the locking condition and the frequency divider divides the clock with division of 255 bit(11111111). After finishing the division, the reference and feedback clock start locking condition with the frequency matching.Then the multiplexer and mixers start removing the spur indicated by yellow strip line as xor_out.thus the spur is reduced at 1000 ns.

IV. Conclusions

The proposed All Digital Phase Locked Loop(ADPLL) design technique is to lock the PLL reference for the frequency matching. The main aim of the proposed technique is to reduce the spur in OFDM. The phase frequency detector is said to be locked when it detects the phase and frequency of the two clock input match. The time to digital convertor is active when phase and frequency mismatch. Then the output of the DCO produced a locking waveform with the allowable frequency. Then the output is excuted by two stage of Multiplexers and Mixers with spur reduction.Using model based approach, this could be tested using Model SIM. As technology progress skew problems will require ADPLLs within the design components to synchronize the clock signal between various blocks. Owing to the flexibility and high performance of digital systems, modems are mainly designed by a digital approach. As fast acquisition is one of the important factors in the design of frequency synthesizers, this digital PLL can be used in mobile applications.

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